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INTEL CORPORATION
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402

EXAMINER	
THAMMAVONG, PRASITH	

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Please find below and/or attached an Office communication concerning this application or proceeding.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/780,330
Filing Date: February 17, 2004
Appellant(s): WOLRICH ET AL.

Robert A. Greenberg
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 15 July 2010 appealing from the Office actions mailed 17 December 2009 and 09 March 2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claim 36-43 are pending, and stand rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay (US Patent # 6,212,604) in view of Sharma (US Patent # 6,055,605). **Claims 1-35 and 44-45** have been cancelled.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

US Patent # 6,212,604	Tremblay	04-2001
US Patent # 6,055,605	Sharma et al.	04-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as

> set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 36-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay (US Patent # 6,212,604) in view of Sharma (US Patent # 6,055,605).

With respect to claim 36, the Tremblay reference teaches a method, comprising:

mapping addresses in a single address space (see fig. 3, shared instruction cache 212) to resources within a set of multiple programmable units (see fig. 3, processors P1 208 and P2 210) integrated within a processor, the single address space including addresses for different ones of the resources (see fig. 3, registers 306 and 312) in different ones of the multiple programmable units; (column 4, lines 7-29, where the system 300 allows for the same instruction(s) stored in instruction cache 212 to access different registers or a different segment of the register files, registers 306 and registers 312, of P1 processor 208 and P2 processor 210 when executed on P1 processor 208 and P2 processor 210, respectively) and

wherein there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units. (column 4, lines 30-58, where there is one-to-one correlation between the registers specified in an instruction and the registers in P1 processor 208 and P2

processor 210 by using an offset, and accordingly, system 300 effectively segments the register files of P1 processor 208 and P2 processor 210 into two segments by setting register index base 302 to 0 (i.e., registers 0 to 127) and register index base 308 to 128 (i.e., registers 128 to 255))

However, the Tremblay reference does not explicitly teach providing data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space.

The Sharma reference teaches that is conventional to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space. (see fig. 1, and column 6, lines 8-15, where there is a shared memory with a single address space shared by a plurality of processors; and column 4, lines 8-39, where each processor has their own private cache for storing data and changes to the data as a result of the memory reference operations are reflected among the entities via the transmission of probe commands in accordance with a conventional cache coherence protocol and where the ordering point requests forwarding of the data from the owner processor to the requesting processor, as required by the memory operation)

The Tremblay and Sharma references are considered analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person having ordinary skill in the art to modify the Tremblay reference to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second one of the multiple programmable units specifying an address within the single address space, as taught by the Sharma reference.

The suggestion/motivation for doing so would have been to improve performance of the multiprocessor system by reducing the latency of inter-reference ordering. (Sharma, column 3, lines 46-60)

Therefore, it would have been obvious to combine the teachings of Tremblay reference with the Sharma reference for the benefit of improving performance as specified in claim 36.

With respect to claim 37, the combination of the Tremblay and Sharma references teaches the method of claim 36, further comprising receiving a command specifying the address in the single address space. (Tremblay, column 4, lines 7-29, where the registers are mapped collectively to an address space)

With respect to claim 38, the combination of the Tremblay and Sharma references teaches the method of claim 37, wherein the command comprises one

selected from the following group: a read command and a write command. (Tremblay, column 7, lines 8-33, where the information is read from and stored into the registers)

With respect to claim 39, the combination of the Tremblay and Sharma references teaches the method of claim 37, wherein the receiving the command comprises receiving the command from a programmable processor. (Tremblay, column 4, lines 7-29, where P2 processor 210 can issue commands as well)

With respect to claim 40, the combination of the Tremblay and Sharma references teaches the method of claim 39, wherein the programmable processor comprises a programmable processor integrated within the processor; and wherein the multiple programmable units comprise multiple programmable engines and the programmable processor. (Tremblay, column 4, lines 7-29, where P1 processor 208 can issue commands as well and where there is registers within the P2 processor 210)

With respect to claim 41, the combination of the Tremblay and Sharma references teaches the method of claim 36, wherein the resources within the set of multiple programmable units comprises register locations within the multiple programmable units. (Tremblay, column 4, lines 7-29, where the registers are programmed with address information)

With respect to claim 42, the combination of the Tremblay and Sharma references teaches the method of claim 36, wherein the single address space comprises addresses corresponding to shared resources external to the multiple programmable units. (Tremblay, column 4, lines 7-29, where the registers store information about the instruction cache and/or main memory)

With respect to claim 43, the combination of the Tremblay and Sharma references teaches the method of claim 36, wherein the multiple programmable units comprise multiple programmable multi-threaded units. (Tremblay, column 6, lines 14-45, where the registers can have multi-threaded instructions within them)

(10) Response to Argument

Appellant's arguments pertaining to claims 36-43

Appellant argues:

Claim 36 recites "mapping addresses in a single address space to resources within a set of multiple programmable units" where the single address space includes "addresses for different ones of the resources in different ones of the multiple programmable units". In particular, there is a "one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units". Claim 36 stands rejected as obvious over Tremblay (U.S. 6,212,604) in view of Sharma (U.S. 6,055,605).

The Advisory Action (mailed 3/9/2010) equates Tremblay's processors P1 and P2 with the recited "multiple programmable units". The action seemingly equates Tremblay's registers 306 and 312 with the recited "resources within in the multiple programmable units". In Tremblay, P1 and P2 both access the same instructions in a shared instruction cache 212. However, a register address of an instruction will identify different registers depending on whether P1 or P2 execute

the instruction. For example, for a given instruction address, P1 will determine a register within P1, while P2 will determine a register within P2 for the same instruction address (col. 4, lines 6-29). The precise register location determined will vary based on the setting of a register index base for each processor, but this does not alter the fact that the same instruction address maps to different registers - a register in P1 and a register in P2. This is simply not the same thing as a "one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units" as recited by claim 36.

Further, Attorney for Applicant, to the extent understood, disagrees with the reasoning presented by the Examiner. For example, the Advisory Action states that "the Tremblay reference teaches the use of a single address space as the registers within the processors are accessing locations in the instruction cache 212 which allows access to the main memory 202". Attorney for Applicant does not agree with this statement nor does Attorney for Applicant understand its relevance. That is, neither instruction cache 212 nor main memory 202 are resources within P1 or P2. Nor does Attorney for Applicant understand registers 306, 312 to access the instruction cache. Instead the registers are accessed in the course of execution of instructions by P1 and P2.

Examiner's Response:

Appellant's arguments have been considered but are not persuasive. The Examiner contends that the Tremblay reference teaches that limitation of *"one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units".* The Tremblay reference teaches (see abstract) a multiprocessor system (e.g., fig. 3, element 206) comprising of processors P1 (e.g., fig. 3, element 208) and P2 (e.g., fig. 3, element 210) accessing a shared instruction cache (e.g., fig. 3, element 212) to allow access to main memory (e.g. element 202). The Tremblay reference also teaches (see column 4, lines 7-29) registers (see fig. 3, elements 306 and 312) are contained within processor P1 and P2, and that the system allows for the same instruction(s) stored in instruction cache 212 to access different registers or a different segment of the register files, registers 306 and registers 312, of P1 processor 208 and P2 processor 210 when executed on P1

processor 208 and P2 processor 210, respectively. The Tremblay reference further teaches (column 4, lines 30-58) the use of an offset to create a one-to-one correlation between the registers specified in an instruction and the registers used by P1 processor 208 and P2 processor 210 during the execution of an instruction, and accordingly, system 300 effectively segments the register files of P1 processor 208 and P2 processor 210 into two segments by setting register index base 302 to 0 (i.e., registers 0 to 127) and register index base 308 to 128 (i.e., registers 128 to 255)). Thus, in the teachings of the Tremblay reference cited above, if P1 processor 208 and P2 processor 210 attempt to access the same location in instruction cache 212, there would be an offset used by P2 processor 210 to access a different location such that there would be a one-to-one correlation between the registers specified in an instruction and the registers used by P1 processor 208 and P2 processor 210 during execution of the instruction, thus teaching the Appellant's limitation of *"one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units".* Thus, the Examiner contends that the Tremblay reference teaches the limitation above as instantly and broadly claimed.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Prasith Thammavong/

Patent Examiner
Art Unit 2187
October 12, 2010

Conferees:

/Brian R. Peugh/

Primary Examiner, Art Unit 2187

/Kevin L Ellis/

Supervisory Patent Examiner, Art Unit 2187